LAKIREDDY BALI REDDY COLLEGE OF ENGINEERING

L.B REDDY NAGAR, MYLAVARAM-521230

R23 REGULATION

SWITCHING THEORY AND LOGIC DESIGN LAB MANUAL

FOR

B. Tech III SEM (ECE)

COURSE CODE: 23EC53

DEPARTMENT OF ECE

2024-2025

STUDENTS GUIDELINES

There are 3 hours allocated to a laboratory session in Switching Theory and Logic Design. It is a necessarypart of the course at which attendance is compulsory.

Here are some guidelines to help you perform the experiments and to submit the reports:

1. Read all instructions carefully and carry them.
2. Ask a demonstrator if you are unsure of anything.
3. Record actual results (comment on them if they are unexpected!)
4. Write up full and suitable conclusions for each experiment.
5. If you have any doubt about the safety of any procedure, contact the demonstrator beforehand.
6. **THINK** about what you are doing!

Breadboard

The breadboard consists of two terminal strips and two bus strips (often broken in the centre). Each bus strip has two rows of contacts. Each of the two rows of contacts is a node. That is, each contact along a row on a bus strip is connected together (inside the breadboard).Bus strips are used primarily for power supply connections, but also used for any node requiring a large number of connections. Each terminal strip has 60 rows and 5 columns of contacts on each side of the centre gap. Each row of 5 contacts as a node.

You will build your circuits on the terminal strips by inserting the leads of circuit components into the contact receptacle and making connections with 22-26 gauge wire. There are wire cutter/strippers and a spool of wire in the lab. It is a good practice to wire
+5V and 0V power supply connections to separate bus strips.

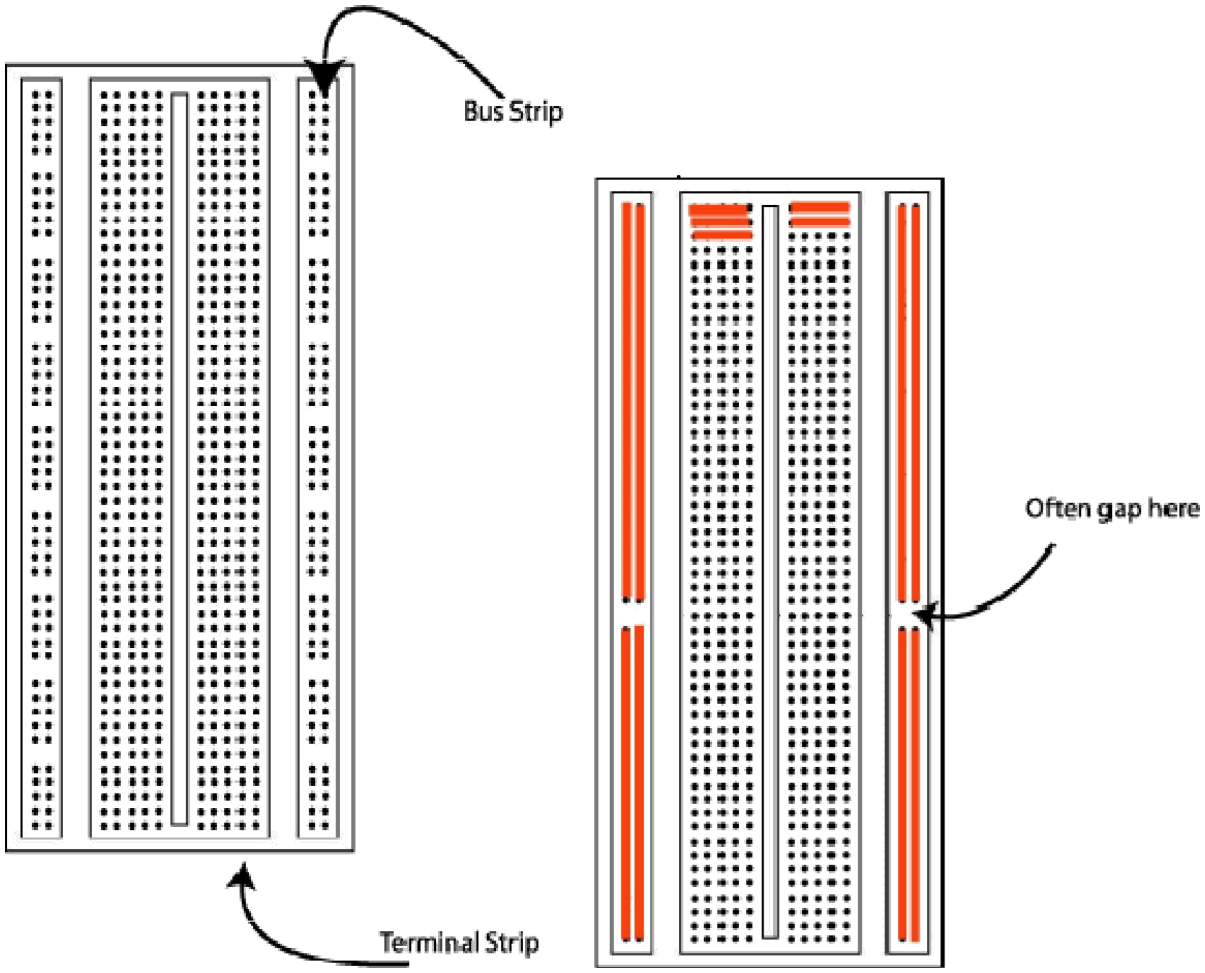


Fig 1: The breadboard, the lines indicate connected holes.

The 5V supply MUST NOT BE EXCEEDED, since this will damage the ICs (Integrated circuits) used during the experiments. Incorrect connection of power to the ICs could result in them exploding or becoming very hot - with the possible serious injury occurring to thepeople working on the experiment! Ensure that the power supply polarity and all components and connections are correct before switching on power.

Building the Circuit:

Throughout these experiments will use IC's to build circuits. The steps for wiring a circuit should be complete in the order described below:

1. Turn the power (Trainer Kit) off before you build anything!
2. Make sure the power is off before you build anything!
3. Connect the +5V and ground (GND) leads of the power supply to the power andground bus strips on your breadboard.
4. Plug the IC's will be using into the breadboard. Point all the IC's in the samedirection with pin 1 at the lower-left corner. (Pin 1 is often identified by a dot or a notch next to it on the chip package)
5. Connect +5V and GND pins of each IC to the power and ground bus strips on thebreadboard.
6. Select a connection on the schematic and place a piece of hook-up wire between corresponding pins of the ICs on the breadboard. It is better to make the short connections before the longer ones.
7. Get one of the group member to check the connections, **before turn the poweron**.
8. If an error is made and is not spotted before turn the power on. Turn the power offimmediately before begin to rewire the circuit.
9. At the end of the laboratory session, collect hook-up wires, ICs and all equipment and return them to the demonstrator.
10. Tidy the area that working and leave it in the same conditionas it was before.

Common Causes of Problems:

1. Not connecting the ground and/or power pins for all ICs.
2. Not turning on the power supply before checking the operation of the circuit.
3. Driving a single gate input with the outputs of two or more gates
4. Modifying the circuit with the power on.

In all experiments will be expect to obtain all instruments/components, leads at the start of the experiment and return them to their proper place after finish the experiment. Please inform the demonstrator/technician any faulty equipment identified. Those who damage any component, inform a demonstrator/ technician, don't put it back in the box of ICs for somebodyelse to use.

Examples of some Logic Gates:

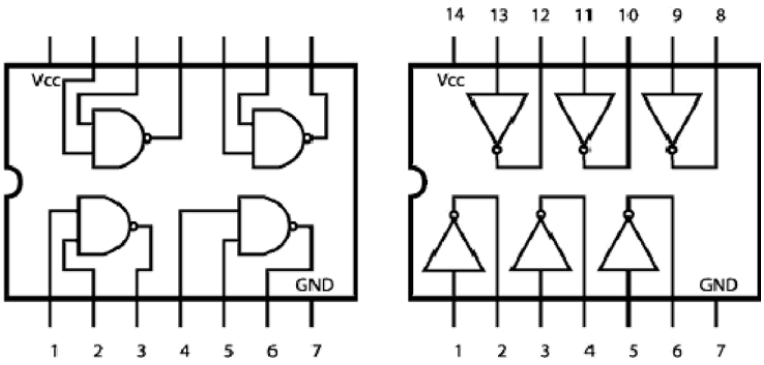


Fig:2: Quad 2 Input 7400 NAND Hex 7404 INVERTER

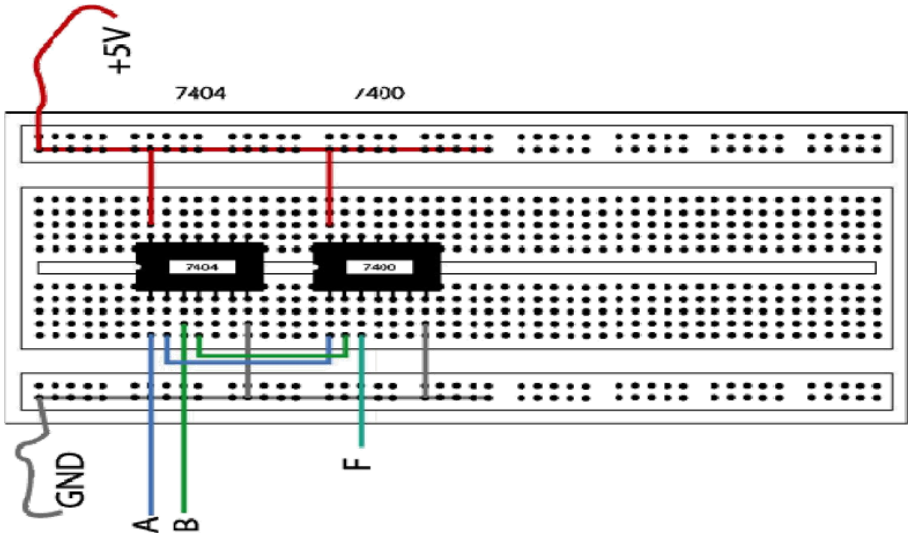


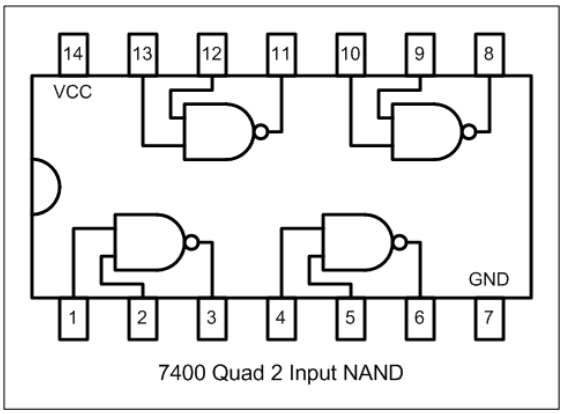
Fig 3: The complete designed and connected circuit.

Sometimes the IC manufacturer may denote the first pin by a small indented circle above the first pin of the IC. Place the IC in the same direction, to save confusion at a later stage. Remember that must connect power to the ICs to get them to work.

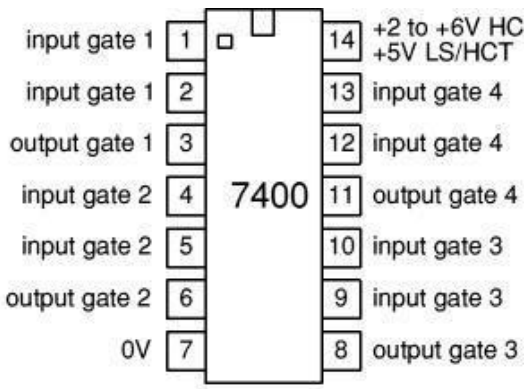
Useful IC Pin details

IC Number	Description of IC
7400	Quad 2 input NAND GATE
7401	Quad 2input NAND Gate (open collector)
7402	Quad 2 input NOR Gate
7403	Quad 2 input NOR Gates (open collector)
7404	Hex Inverter
7408	Quad 2 input AND gate
7421	Dual 4 input AND Gates
7430	8 input NAND Gate
7432	Quad 2 input OR Gates
7486	Quad 2 input EX-OR Gates
74107	Quad 2 input EX-OR Gates
74109	Dual j-k Flip Flops
74173	Quad D Flip Flops
74174	Hex D Flip Flops
7473	Dual j-k Flip Flops, asynchronous clear
7474	Dual D Flip Flops
7475	Quad Bi-stable latch
7476	Dual j-k Flip Flops, asynchronous preset and clear

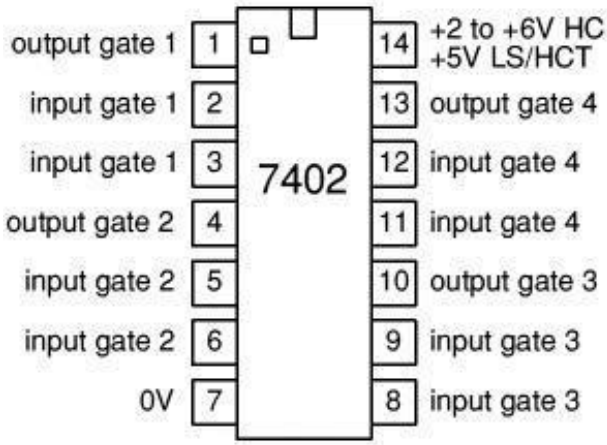
7400(NAND)



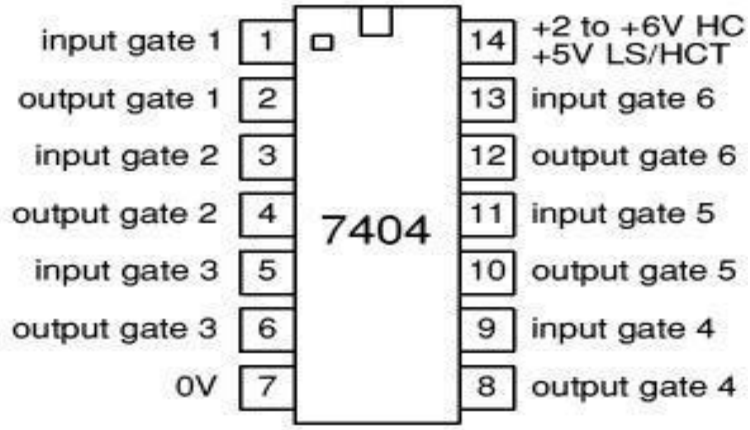
7400 Quad 2 Input NAND



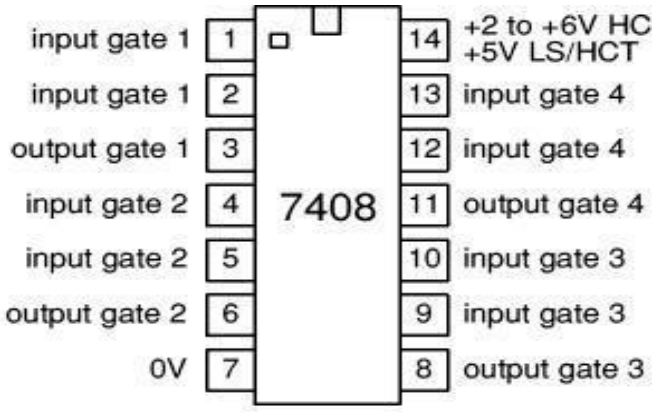
7402(NOR)



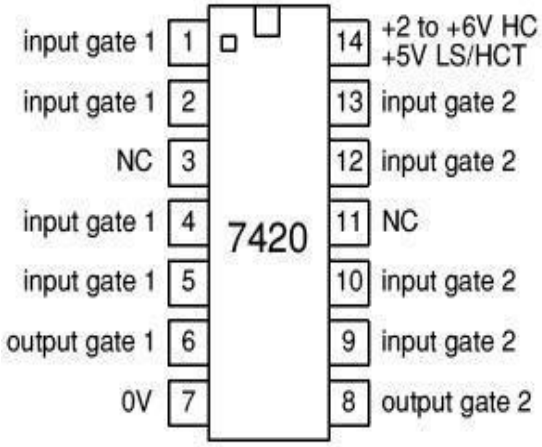
7404(NOT)



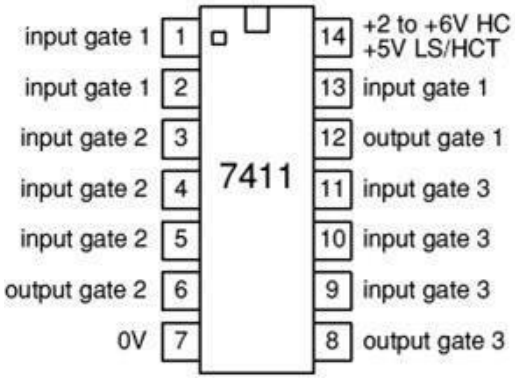
7408(AND)



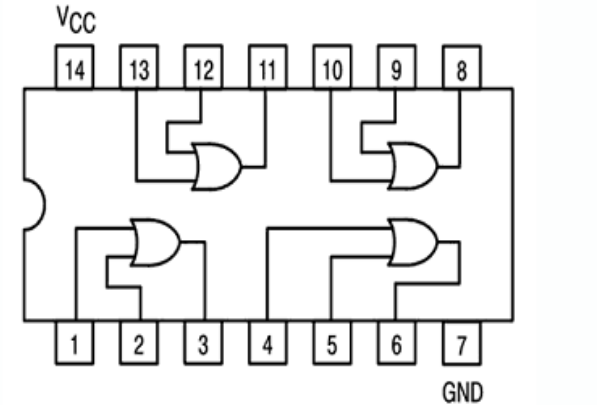
7420(4-i/p NAND)



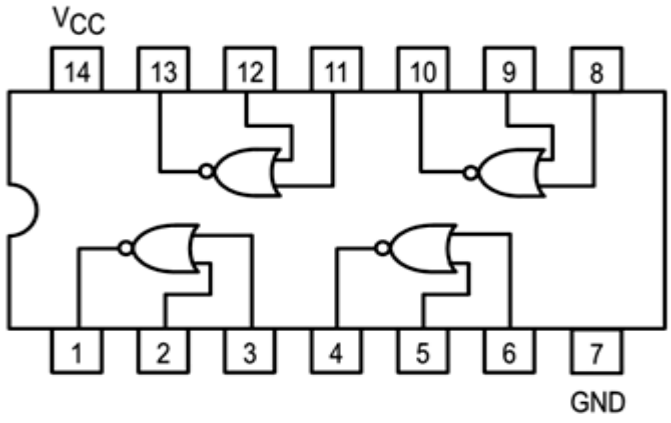
7411(3-i/p AND)



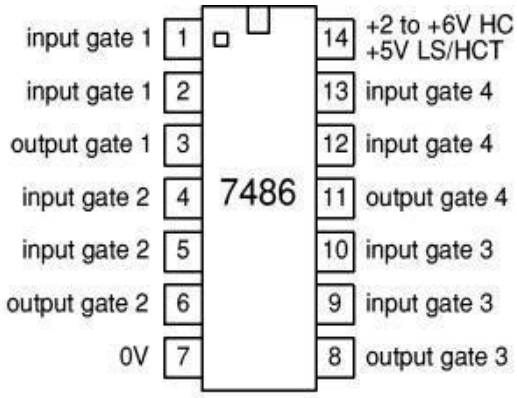
7432(OR)

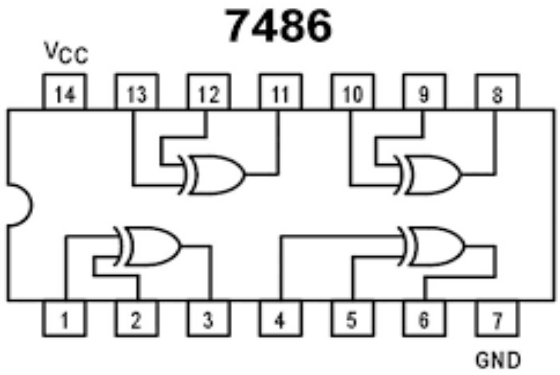


7402(NOR)

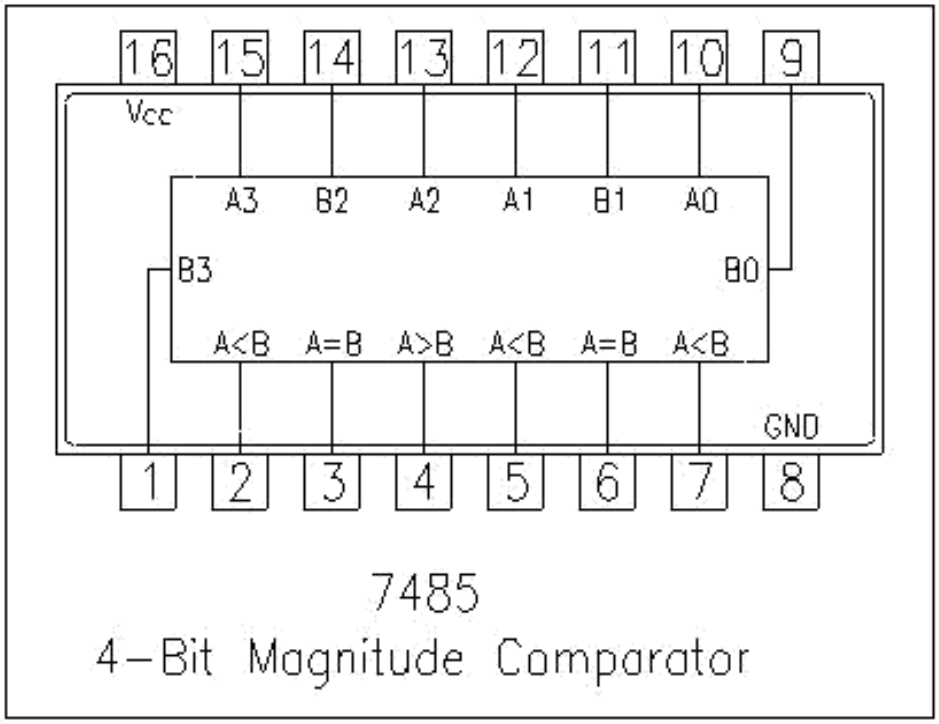


7486(EX-OR)

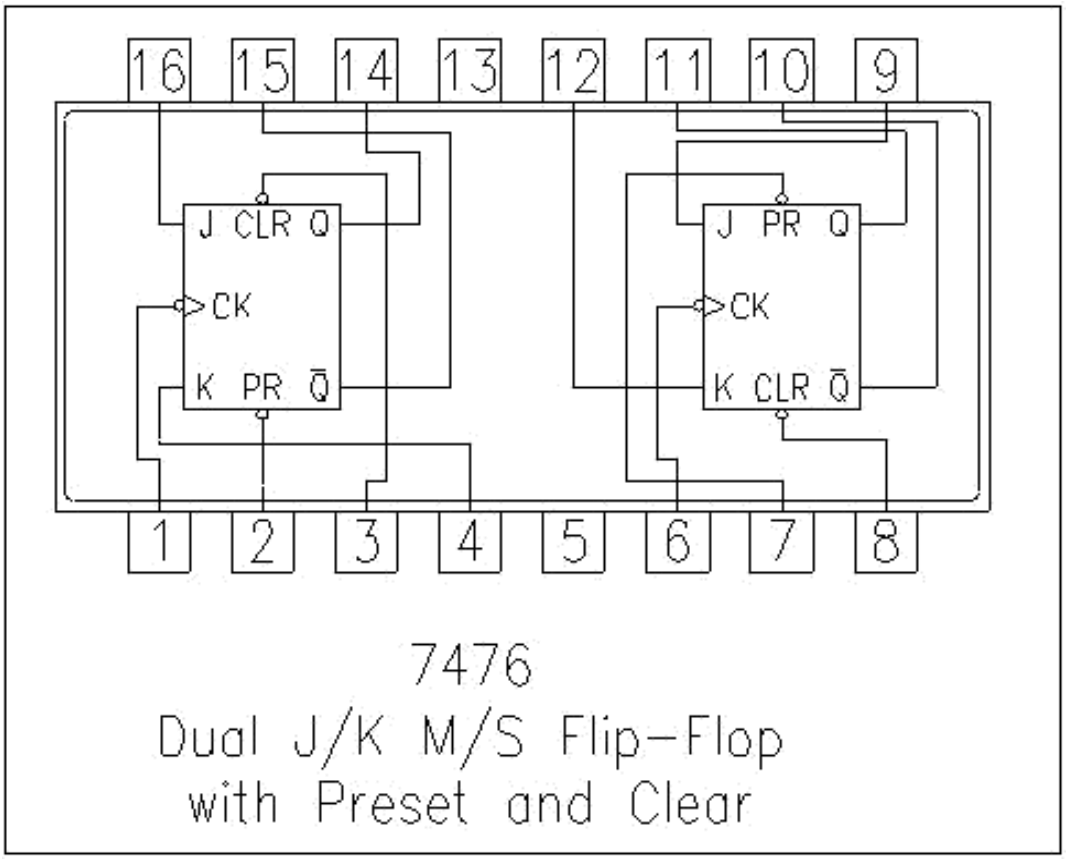




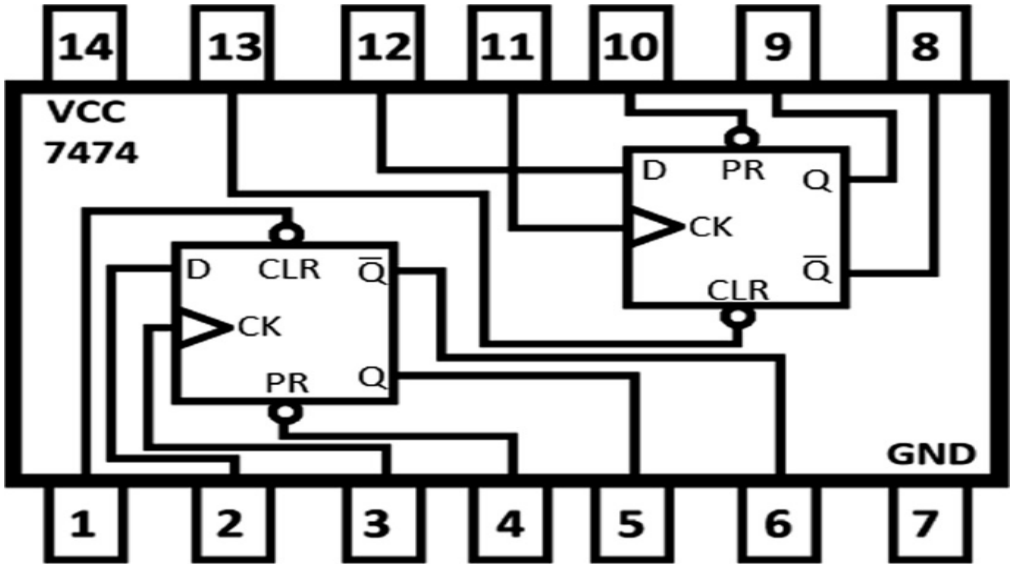
(7485-4 bit Comparator)



(7476-Dual JK-F/F)



(7474 Dual D-F/F)



LIST OF EXPERIMENTS

S.No	Name of the Experiment	Page No
1.	Implementation of following Logic gates using universal gates. (i) OR (ii) AND (iii) NOT (iv) Exclusive-OR (v) EX-NOR	
2.	Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital Trainer Kit.	
3.	Verification of functional table of 3 to 8-line Decoder /De-multiplexer	
4.	4 variable logic function verification using 8 to1 multiplexer.	
5.	Design full adder circuit and verify its functional table.	
6.	Verification of functional tables of (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip–Flop (iii) D Flip-Flop	
7.	Design a four-bit ring counter using D Flip–Flops/JK Flip Flop and verify output.	
8.	Design a four-bit Johnson's counter using D Flip-Flops/JK Flip Flops and verify output.	
9.	Verify the operation of 4-bit Universal Shift Register for different Modes of operation.	
10.	Draw the circuit diagram of MOD-8 ripple counter and construct a circuit using T-Flip- Flops and Test It with a low frequency clock and sketch the output waveforms.	
11.	Design MOD–8 synchronous counter using T Flip-Flop and verify the result and sketch the output waveforms.	
12.	(a) Draw the circuit diagram of a single bit comparator and test the output (b) Construct 7 Segment Display Circuit Using Decoder and7 Segment LED and test it.	

Additional Experiments:

1. Design BCD Adder Circuit and Test the Same using Relevant IC
2. Design Excess-3 to 9- Complement convertor using only four Full Adders and test the Circuit.
3. Design an Experimental model to demonstrate the operation of 74154 De-Multiplexer using LEDs for outputs.
4. Design of any combinational circuit using Hardware Description Language
5. Design of any sequential circuit using Hardware Description Language.

EXP.NO:01 **DATE:**

LOGIC GATES

AIM: Implementation of following Logic gates using universal gates.

(i) OR (ii) AND (iii) NOT (iv) Exclusive-OR (v) EX-NOR

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS08,74LS32,74LS04 74LS00,74LS02,74LS86, 74LS266	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

The basic logic gates are the building blocks of more complex logic circuits. These logic gates perform the basic Boolean functions, such as AND, OR, NAND, NOR, Inversion, Exclusive-OR, Exclusive-NOR. Fig. below shows the circuit symbol, Boolean function, and truth. It is seen from the Fig that each gate has one or two binary inputs, A and B, and one binary output, C. The small circle on the output of the circuit symbols designates the logic complement. The AND, OR, NAND, and NOR gates can be extended to have more than two inputs. A gate can be extended to have multiple inputs if the binary operation it represents is commutative and associative.

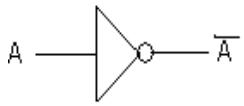
PROCEDURE:

1. Do the Connections as per symbol and indent marked on PCB.
2. Give the logic input to the gate under test as per symbol from INPUT
3. SWITCHES section.
4. Connect output of gate under test to any of the led from OUTPUT LED section
5. Observe the output on LEDS from OUTPUT SECTION and verify the truth table.

LOGIC DIAGRAMS:

NOT GATE

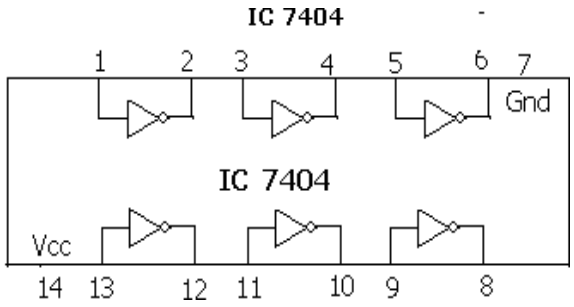
SYMBOL



TRUTH TABLE

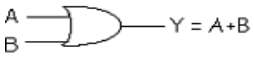
Dec	I/P (A)	O/P $\overline{(A)}$
0	0	1
1	1	0

IC 7404



OR GATE

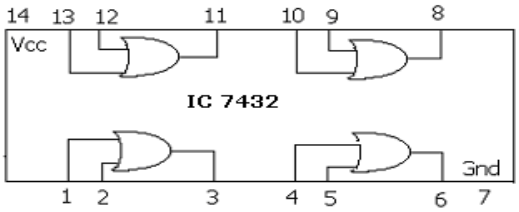
SYMBOL



TRUTH TABLE

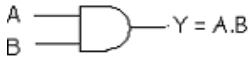
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	1

IC 7432



AND GATE

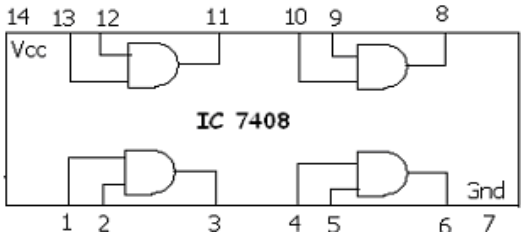
SYMBOL



TRUTH TABLE

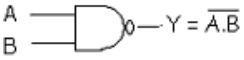
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	0
2	1	0	0
3	1	1	1

IC 7408



NAND GATE

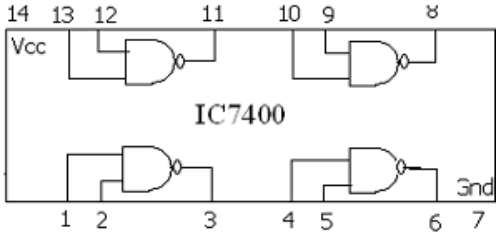
SYMBOL



TRUTH TABLE

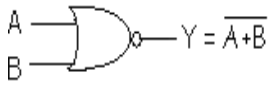
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	1
2	1	0	1
3	1	1	0

IC 7400



NOR GATE

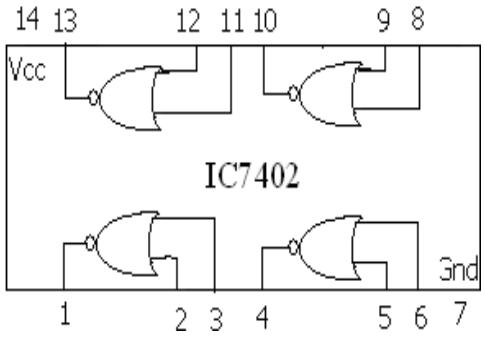
SYMBOL



TRUTH TABLE

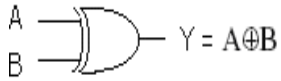
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	1
1	0	1	0
2	1	0	0
3	1	1	0

IC7402



EX-OR GATE

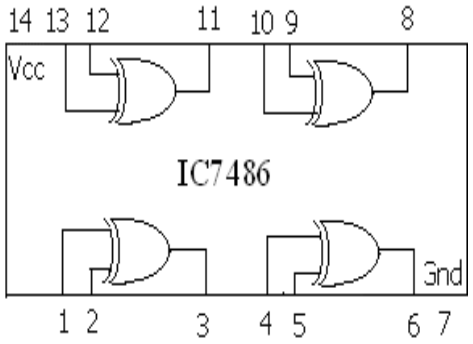
SYMBOL

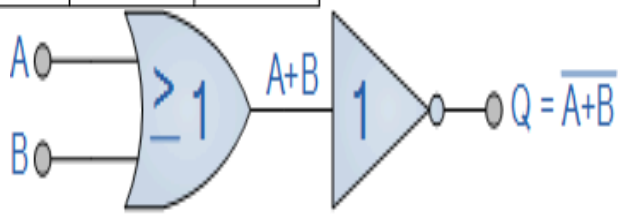


TRUTH TABLE

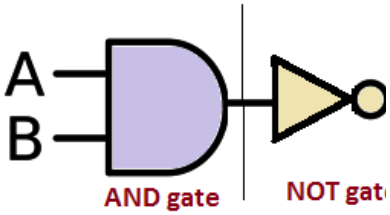
Dec Eq	Inputs		Output
	A	B	Y
0	0	0	0
1	0	1	1
2	1	0	1
3	1	1	0

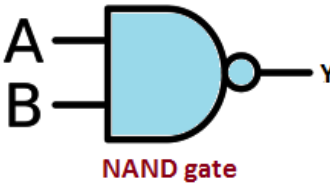
IC- 7486

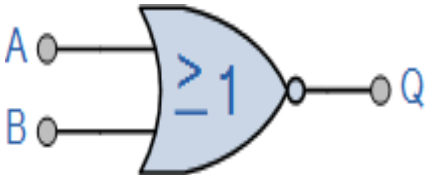




2-input "OR" gate plus a "NOT" gate



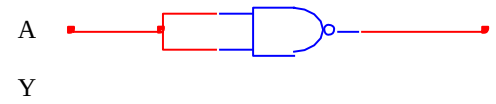




NOR gate

NOT-Gate:

TRUTH TABLE:

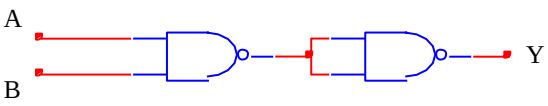


Truth Table

A	Y
0	
1	

AND-Gate:

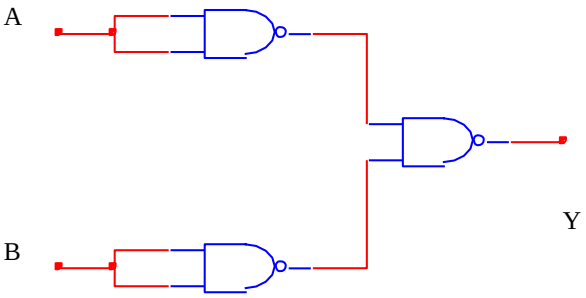
Truth Table:



Truth Table

A	B	Y
0	0	
0	1	
1	0	
1	1	

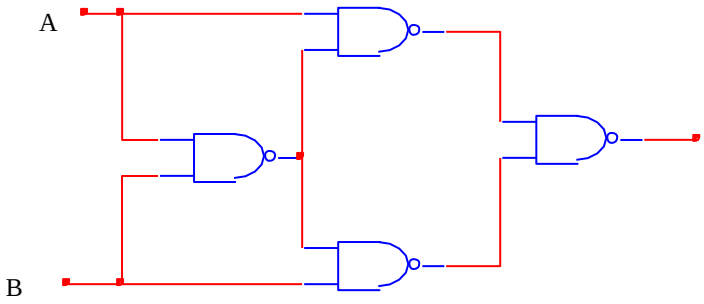
OR-Gate:



Truth Table:

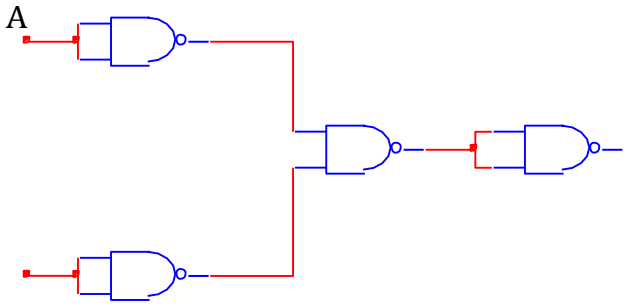
A	B	Y
0	0	
0	1	
1	0	
1	1	

EX-OR Gate:



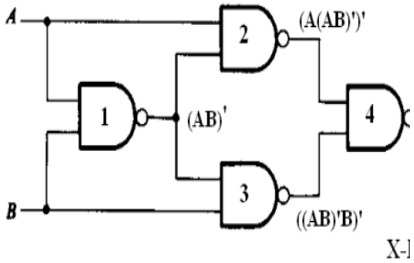
A	B	Y
0	**0**	
0	**1**	
1	**0**	
1	**1**	

NOR Gate:



A	**B**	**Y**
0	0	
0	1	
1	0	
1	1	

NAND Gates as EX-NOR Gate



A	**B**	**Y**
0	0	
0	1	
1	0	
1	1	

X-

Procedure:

1. Connect the logic gates as shown in the diagrams.
2. Feed the logic signals 0(0V) or 1(5V) from the logic input switches indifferent combinations at the inputs A & B.
3. Monitor the output using logic output LED indicators
4. Repeat steps 1 to 3 for NOT, AND, OR, EX – OR & EX-NOR operationsand compare the outputs with the truth tables.

Precautions:

1. All the connections should be made properly.
2. IC should not be reversed.

Result:

VIVA QUESTIONS:

1) What are the universal logic gates?
2) Define Positive logic and Negative Logic.
3) What are the basic logic elements?
4) What is different between Ex-or & Ex-nor gate?
5) Draw the EX-NOR by using the NAND gate.

EXP.NO:02 **DATE:**

Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital Trainer kit.

AIM:- To Design a simple combinational circuit with four variables and obtain minimal SOP expression and verify the truth table using Digital Trainer kit.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS08,74LS32,74LS04,	1 (Each)
2	Digital IC Trainer Kit	If required	1
3	Patch cards		As per required
4	Fixed Power Supply	(0-5v)	1

THEORY:

Combinational Logic Circuits are made up from basic logic NAND, NOR or NOT gates that are "combined" or connected together to produce more complicated switching circuits. These logic gates are the building blocks of combinational logic circuits.

An example of a combinational circuit is a decoder, which converts the binary code data present at its input into a number of different output lines, one at a time producing an equivalent decimal code at its output.

Combinational logic circuits can be very simple or very complicated and any combinational circuit can be implemented with only NAND and NOR gates as these are classed as "universal" gates.

The three main ways of specifying the function of a combinational logic circuit are:

- 1. Boolean Algebra – This forms the algebraic expression showing the operation of the logic circuit for each input variable either True or False that results in a logic "1" output.
- 2. Truth Table – A truth table defines the function of a logic gate by providing a concise list that shows all the output states in tabular form for each possible combination of input variable that the gate could encounter.
- 3. Logic Diagram – This is a graphical representation of a logic circuit that shows the wiring and connections of each individual logic gate, represented by a specific graphical symbol, that implements

the logic circuit.

4. The Sum of Product Form

In the sum of the product form of representation, The product num is logical and operation of the different input variables where the variables could be in the true form or in the complemented form.In SOP sum refers to logical OR Operation. Therefore, in this sum of product form of expression, we perform logical or operations on different product terms. Therefore it is known as the Sum of Product form.

Consider a four variable Boolean expression and simplify it into minimum literals.

Ex:

$$F = A + B[AC + (B + \bar{C})D]$$

Draw the Logic diagram for given Boolean function:

Draw the Logic diagram for simplified Boolean function:

Truth Table:

\

S.No.	A	B	C	D	F	Fs
1	0	0	0	0		
2	0	0	0	1		
3	0	0	1	0		
4	0	0	1	1		
5	0	1	0	0		
6	0	1	0	1		
7	0	1	1	0		
8	0	1	1	1		
9	1	0	0	0		
10	1	0	0	1		
11	1	0	1	0		
12	1	0	1	1		
13	1	1	0	0		
14	1	1	0	1		
15	1	1	1	0		
16	1	1	1	1		

PROCEDURE:

1. Construct the logic diagram for the given Boolean expression.
2. Provide the input combinations to the logic diagram
3. Note down the output value in the Truth Table
4. Construct the logic diagram for simplified expression.
5. Repeat the step 3.

Precautions:

1. All the connections should be made properly.
2. IC should not be reversed.

Result:

VIVA QUESTIONS:

1. What is the need for simplification of Boolean expression?
2. Define De-Morgan's theorem
3. Define the terms i) SSOP ii) SPOS
4. Define Consensus theorem.
5. Define combinational logic circuit.

EXP.NO:03 **DATE:**

3 TO 8-LINE DECODER /DE-MULTIPLEXER

AIM:- To Verification Of Functional Table Of 3 To 8-Line Decoder /De-Multiplexer

.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	74LS138	1
2	Digital IC Trainer Kit	If Required	1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

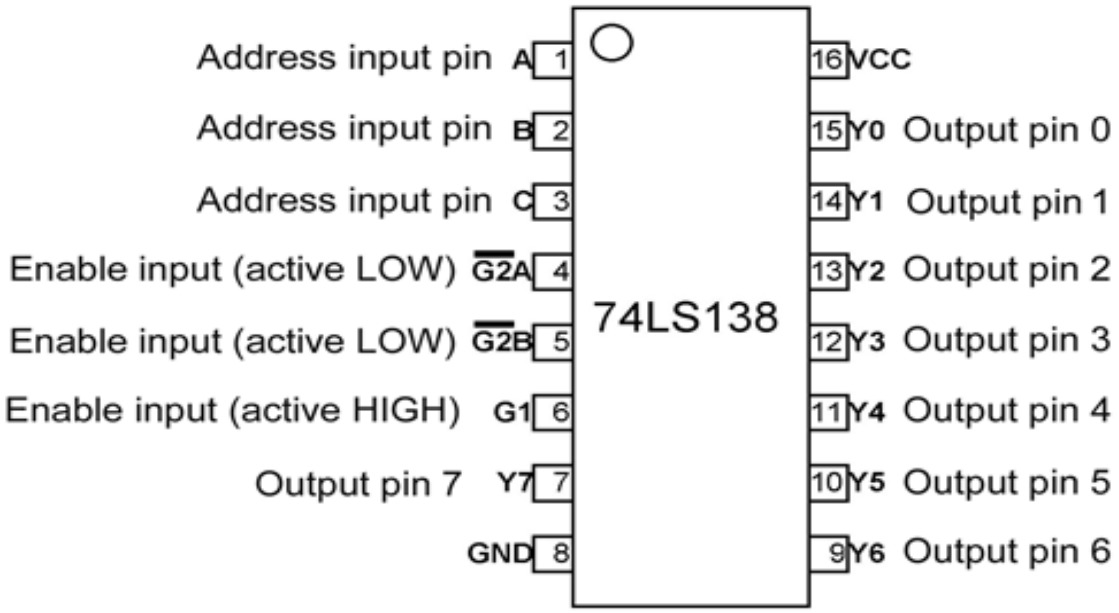
THEORY DECODER:

A decoder is a device which does the reverse operation of an encoder, undoing the encoding so that the original information can be retrieved. The same method used to encode is usually just reversed in order to decode. It is a combinational circuit that converts binary information from n input lines to a maximum of 2^n unique output lines. In digital electronics, a decoder can take the form of a multiple-input, multiple-output logic circuit that converts coded inputs into coded outputs, where the input and output codes are different. e.g. n-to-2^n, binary-coded decimal decoders. Enable inputs must be on for the decoder to function, otherwise its outputs assume a single "disabled" output code word. In case of decoding all combinations of three bits eight (2^3=8) decoding gates are required. This type of decoder is called 3-8 decoder because 3 inputs and 8 outputs. For any input combination decoder outputs are 1.

Procedure:

1. The truth table and a design of 3:8 decoder are given.
2. Realize this circuit on your board by using logic circuit.
3. Connect three inputs x,y,z to the switches & eight outputs vice-versa.
4. Connect the functions outputs to LEDs.
5. Verify input/output relation (Truth table) of this converter.

IC74138 Pin Description Circuit connection



DEMULTIPLEXER:

The function of Demultiplexer is in contrast to multiplexer function. It takes information from one line and distributes it to a given number of output lines. For this reason, thedemultiplexer is also known as a data distributor. Decoder can also be used as demultiplexer. In the 1: 4 demultiplexer circuit, the data input line goes to all of the AND +9gates. Thedata select lines enable only one gate at a time and the data on the data input line will pass through the selected gate to the associated data output line.

TRUTH TABLE FOR DEMUX:

INPUTS						OUTPUTS							
G1	G2A	G2B	A (MSB)	B	C (LSB)	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	1	X	X	X								
X	1	X	X	X	X								
0	X	X	0	0	0								
1	0	0	0	0	1								
1	0	0	0	1	0								
1	0	0	0	1	1								
1	0	0	1	0	0								
1	0	0	1	0	1								
1	0	0	1	1	0								
1	0	0	1	1	1								

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the power supply.
2. Apply proper logic inputs o the Demultiplexer and observe the output on LEDs.
3. Verify the function table of Demultiplexer.

PRECAUTIONS:

1) Make the connections according to the IC pin diagram.
2) The connections should be tight.
3) The Vcc and ground should be applied carefully at the specified pin only.

RESULT:

VIVA QUESTIONS:

1. What do you understand by decoder?
2. What is demultiplexer?
3. What do you understand by encoder?
4. What is the main difference between decoder and demultiplexer?
5. Why Binary is different from Gray code?

EXP NO:04 **DATE:**

VARIABLE LOGIC FUNCTION VERIFICATION USING 8 TO1 MULTIPLEXER.

AIM: To Verify the Variable Logic Function Verification Using 8 To1 Multiplexer.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 74153	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

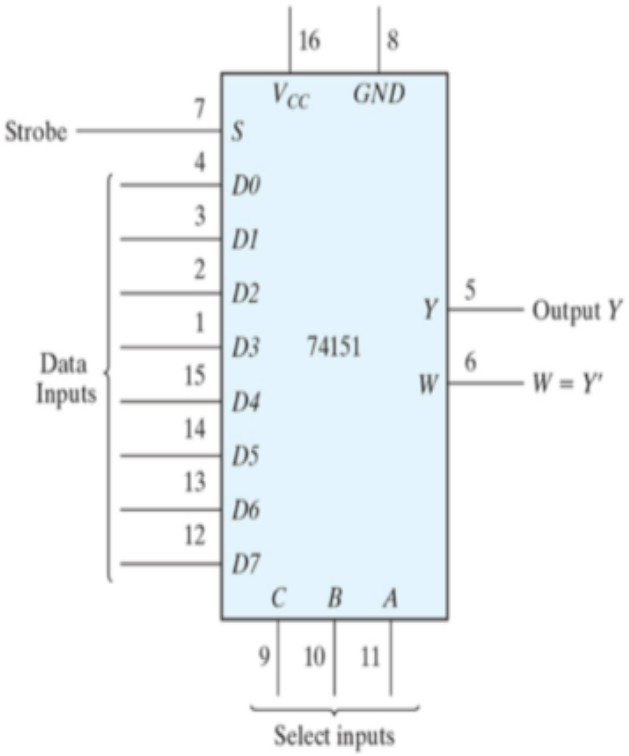
The Multiplexers or data selector is a logic circuit that selects one out of several inputs to a single output. The input selected is controlled by a set of select lines. For selecting one output line from n-input lines, a set of m-select lines is required. The relationship between the number of input lines and the select lines is given by $2^m = n$.

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the powersupply.
2. Apply proper logic inputs o the Multiplexer and observe the output on LEDs.
3. Verify the function table of multiplexer in both the cases.

BLOCK DIAGRAM OF 8:1 MUX & FUNCTION TABLE

Figure 1: 74151 IC: 8x1 mux



TRUTH TABLE

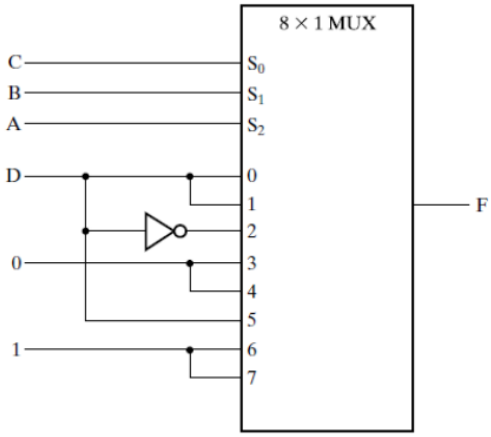
$\overline{E}$	S_2	S_1	S_0	I_0	I_1	I_2	I_3	I_4	I_5	I_6	I_7	$\overline{Z}$	Z
H	X	X	X	X	X	X	X	X	X	X	X	H	L
L	L	L	L	L	X	X	X	X	X	X	X	H	L
L	L	L	L	H	X	X	X	X	X	X	X	L	H
L	L	L	H	X	L	X	X	X	X	X	X	H	L
L	L	L	H	X	H	X	X	X	X	X	X	L	H
L	L	H	L	X	X	L	X	X	X	X	X	H	L
L	L	H	L	X	X	H	X	X	X	X	X	L	H
L	L	H	H	X	X	X	L	X	X	X	X	H	L
L	L	H	H	X	X	X	H	X	X	X	X	L	H
L	H	L	L	X	X	X	X	L	X	X	X	H	L
L	H	L	L	X	X	X	X	H	X	X	X	L	H
L	H	L	H	X	X	X	X	X	L	X	X	H	L
L	H	L	H	X	X	X	X	X	H	X	X	L	H
L	H	H	L	X	X	X	X	X	X	L	X	H	L
L	H	H	L	X	X	X	X	X	X	H	X	L	H
L	H	H	H	X	X	X	X	X	X	X	L	H	L
L	H	H	H	X	X	X	X	X	X	X	H	L	H

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

- Multiplexer implementation of 4-Variable function

$$F(A,B,C,D) = \Sigma m(1,3,4,11,12,13,14,15)$$

A	B	C	D	F	
0	0	0	0	0	F = D
0	0	0	1	1	
0	0	1	0	0	F = D
0	0	1	1	1	
0	1	0	0	1	$F = \overline{D}$
0	1	0	1	0	
0	1	1	0	0	F = 0
0	1	1	1	0	
1	0	0	0	0	F = 0
1	0	0	1	0	
1	0	1	0	0	F = D
1	0	1	1	1	
1	1	0	0	1	F = 1
1	1	0	1	1	
1	1	1	0	1	F = 1
1	1	1	1	1	



RESULT :

VIVA QUESTIONS:

1. What is a multiplexer?
2. What are the applications of multiplexer and de-multiplexer?
3. What is a de-multiplexer?
4. In 2n to 1 multiplexer how many selection lines are there?
5. Implement an 8:1 mux using 4:1 muxes?

Exp No: 05 DESIGN FULL ADDER CIRCUIT AND VERIFY ITS FUNCTIONAL TABLE

Date:

AIM: To Design full adder circuit and verify its functional table.

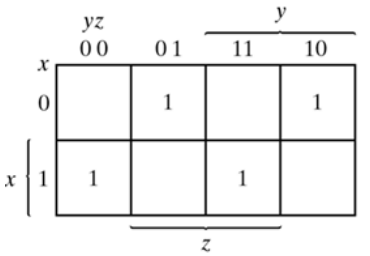
APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC's	74LS08, 74LS32, 74LS04, 74LS00, 74LS02, 74LS86	1
2	Patch Chords		REQUIRED
3	Fixed Power Supply	(0-5V)	1
4	Digital IC Trainer Kit		1

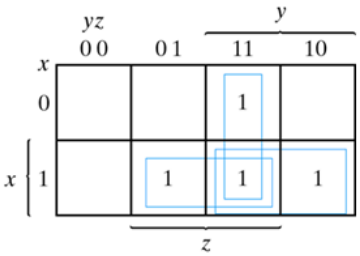
THEORY:

Full adder

A Full adder is a combinational circuit that performs addition of three input bits. Half adder has inputs X, Y, Z and outputs sum (S) and carry(C). The simplified Boolean expressions are

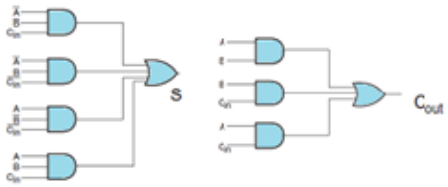


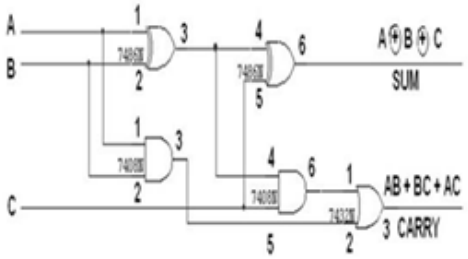
$S = x'y'z + x'yz' + xy'z' + xyz$



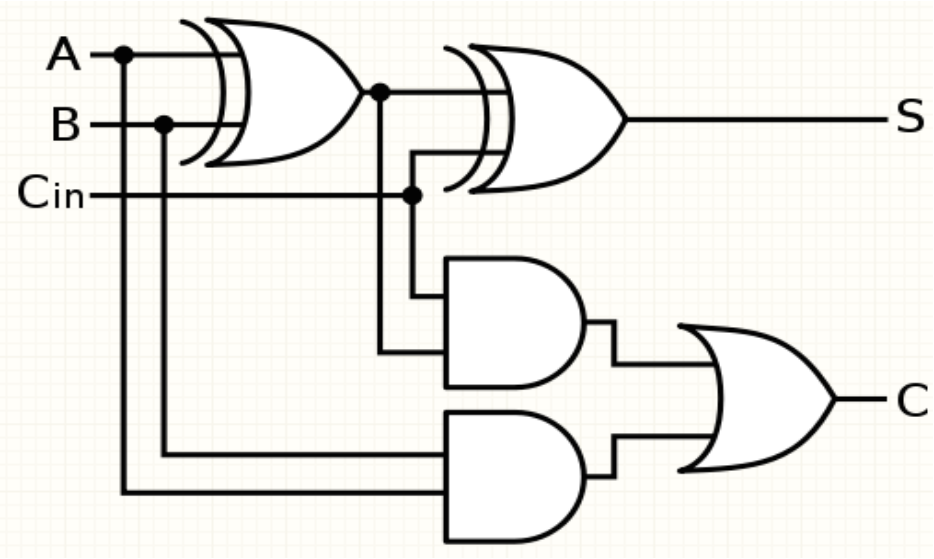
$C = xy + xz + yz$
$= xy + xy'z + x'yz$

BLOCK DIAGRAM OF FULLADDER & TRUTH TABLE





A	B	C_{in}	SUM (S)	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1



INPUTS			OUTPUTS	
A	**B**	**C**	**SUM**	**CARRY**

PROCEDURE:

1. Connect A, B and C I/P of Full adder to switches from input switches section.
2. Connect SUM & CARRY O/P of Full Adder to LEDs from O/P LED section.
3. Switch ON the power supply of the Kit.
4. Provide proper inputs to Full adder using switches as per truth table of Full adder shownabove.
5. Observe the O/P of Full Adder on LEDs.
6. Verify the functionality of Full Adder as per truth table & Note it down.

RESULT:

VIVA QUESTIONS:

1. What is use of Full adder?
2. What is difference between the half and full adder?
3. How many half adders required to make a full adder?
4. In full adder how many types of gates are required?
5. Draw full adder circuit?

Exp No: 06 **Date:**

JK Edge triggered Flip–Flop, JK Master Slave Flip–Flop & D Flip-Flop

AIM: Verification of functional tables of (i) JK Edge triggered Flip–Flop (ii) JK Master Slav Flip– Flop (iii) D Flip-Flop

APPARATUS REQUIRED:

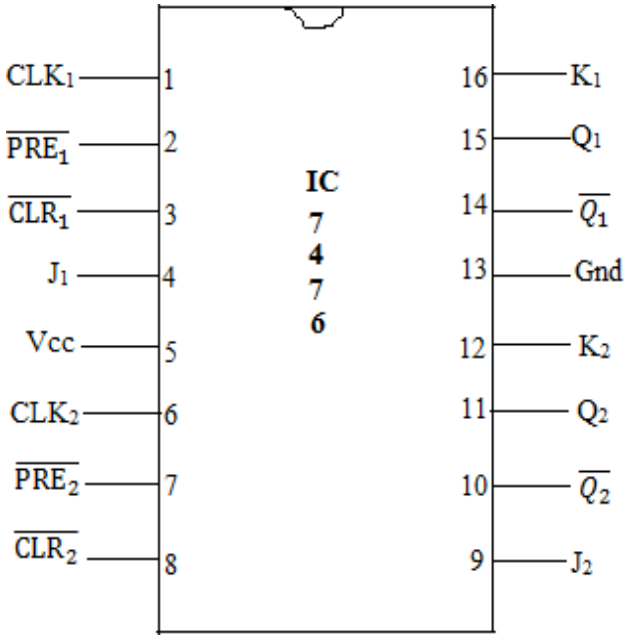
S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7476,74107,7474	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY: Basically Flip-Flops are the bistable multivibrators that stores logic 1 and logic 0.Shift registers, memory, and counters are built by using Flip – Flops. Any complex sequential machines are build using Flip – Flops. Sequential circuit (machine) output depends on the present state and input applied at that instant.

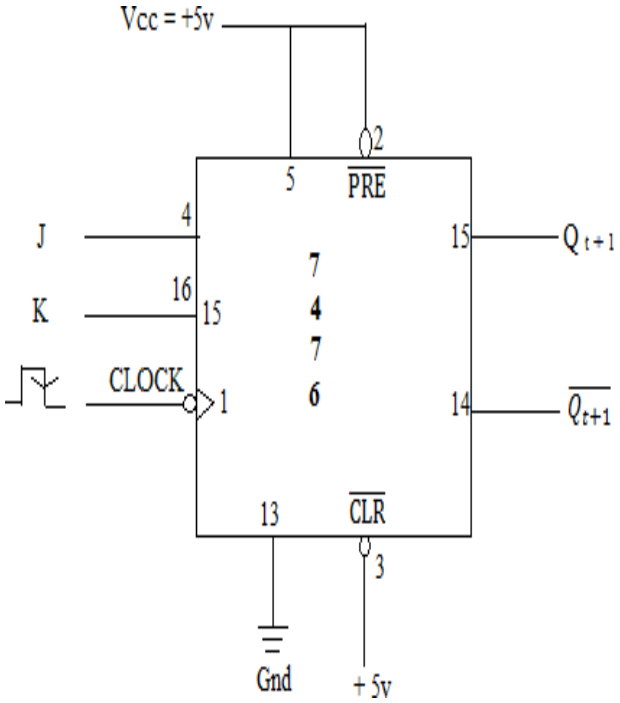
Mealy Machine is one whose output depends on both the present state and the input. Moore machines one whose output depends only on the present state of the sequential circuit. Note that the truth table of J – K Flip – Flop is same as the Master – Slave.

J – K Flip Flop and they must be remain same because IC – 7476is –ve edge trigged flip – flop and we know that race around condition is eliminated by edge triggered flip – flop. Another way of eliminating race around condition is by using Master – Slave J –K Flip – Flop. When J = K = 1 (logic HIGH), J – K Flip – Flop changes output many times for single clock pulse, it is Smaller than width of the clock pulse.

i) Implementation of JK Flip-Flop Design:



Pin diagram of 7476



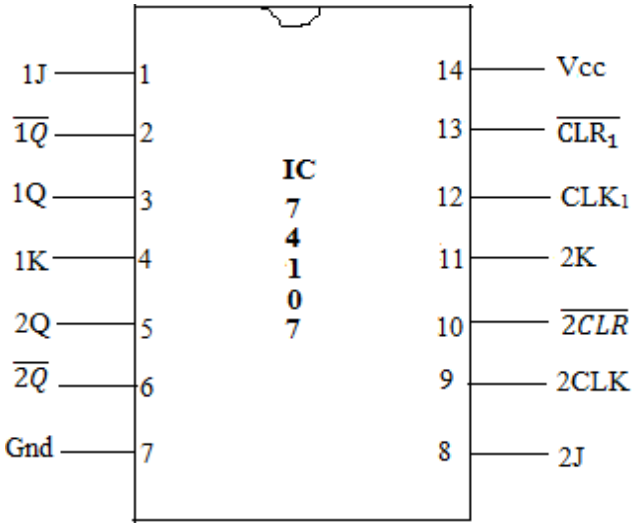
Block Diagram of JK Flip -Flop

Truth Table of JK Flip – Flop

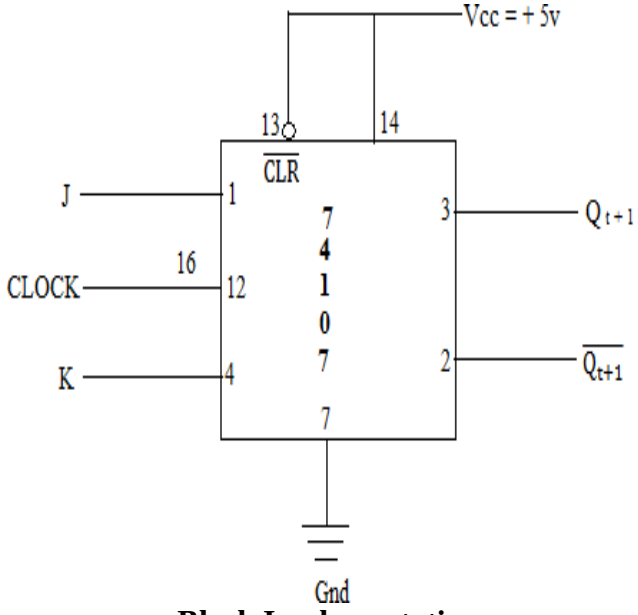
Inputs			Output (Expected)	Output (Actual)
Q	**J**	**K**	**Qn_{+1}**	**Qn_{+1}**
0	0	0	0	
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	

ii) Master Slave JK Flip – Flop:

IC – 74107: Dual – Master – Slave JK Flip-Flop



PIN OUT Diagram



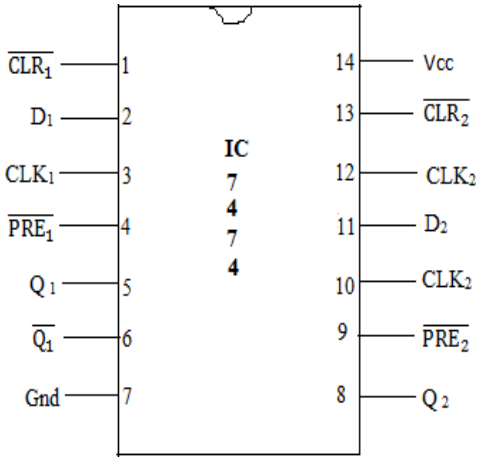
Block Implementation

Truth Table of JKMS Flip – Flop:

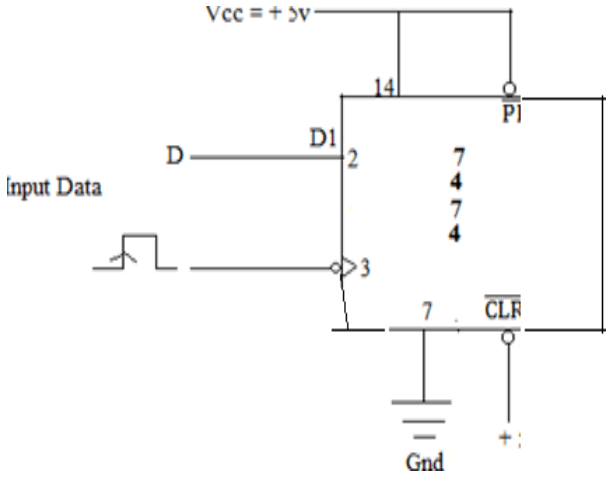
Inputs			Outputs	
Q	J	K	Q_{n+1} (Expected)	Q_{n+1} (Actual)
0	0	0	0	
0	0	1	0	
0	1	0	1	
0	1	1	1	
1	0	0	1	
1	0	1	0	
1	1	0	1	
1	1	1	0	

iii) D Flip – Flop:

IC – 7474: Dual + ve edge triggered D Flip-Flop:



PINOUT Diagram



Block Implementation

Truth Table of D Flip – Flop:

Inputs		Outputs
Q	D	Q_{t+1}
0	0	0
0	1	1
1	0	0
1	1	1

PROCEDURE:

JK FLIP_FLOP:

1. Connect PR to **PRESET**, CR to **CLEAR** and J and K terminals to the logic input switches.
2. Connect CLK of JK flip-flop to Clock terminal.
3. Connect Q and /Q terminals to LED indicators in O/P section.
4. Set the PR, CR, CLK, J and K Signals by means of the switches as per the truth table of JK flip-flop given above and verify the Q and /Q outputs by changing possible input condition.

JKMS FLIP-FLOP:

1. Do the connection for MS JK Flip-Flop as shown in above.
2. Connect PR to **PRESET**, CR to **CLEAR** of both the flip-flops and J and K terminals of master flip-flop to the logic input switches.
3. Connect CLK of master JK flip-flop to Clock terminal.
4. Connect Q and /Q terminals of slave flip-flop to LED indicators in O/P LED section. Also connect Q & /Q terminals of master flip-flop to the LEDs in O/P

LED section.

5. Set the PR, CR, clk, J and K Signals by means of the switches as per the truth table of MS JK flip-flop given above and verify the Q and /Q outputs.

D FLIP-FLOP:

1. Connect PR to **PRESET**, CR to **CLEAR** and D terminals to the logic input switch.
2. Connect the CLK of D Flip-Flop to CLOCK terminal.
3. Connect Q and /Q terminals to LED indicators in O/P LED section.
4. Set the PR, CR, CLK and D Signals by means of the switches as per the truth table of D flip- flop given above and verify the Q and /Q outputs.

RESULT:

VIVA QUESTIONS:

1. What is flip-flop?
2. How many types of flip -flop are used?
3. What is the characteristic equation for T flip-flop?
4. What is full form of T flip-flop?
5. Which Gates are used in SR flip flops to a JK flip-flop?

Exp No: 07 **Date:**

Ring Counter

AIM: Design a four-bit ring counter using D Flip–Flops/JK Flip Flop and verify output.

Apparatus Required:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7474	4
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Power Supply	(0-5v)	1

Theory:

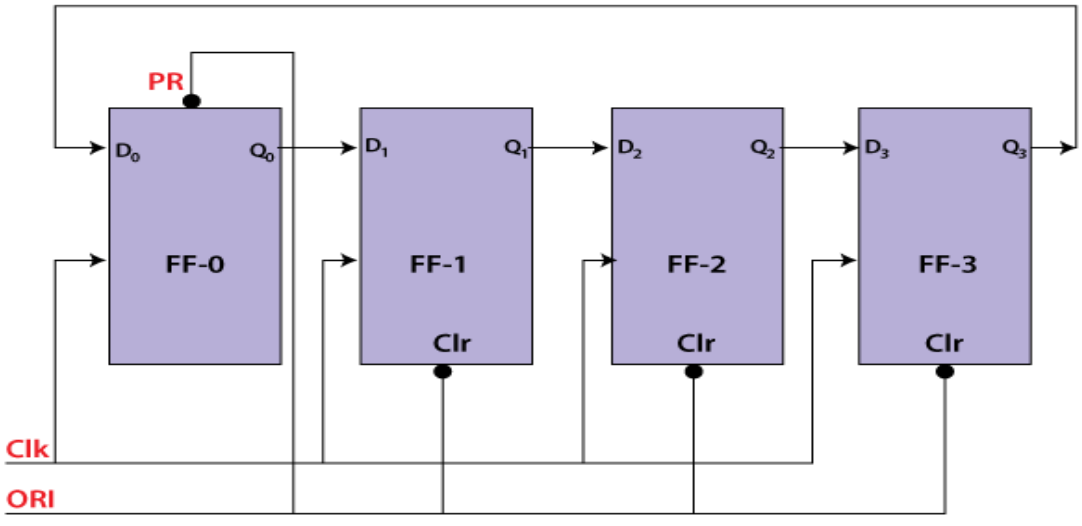
A ring counter is a special type of application of the Serial IN Serial OUT Shift register. The only difference between the shift registers and the ring counter is that the last flip flop outcome is taken as the output in the shift register. But in the ring counter, this outcome is passed to the first flip flop as an input. All of the remaining things in the ring counter are the same as the shift register.

In the Ring counter

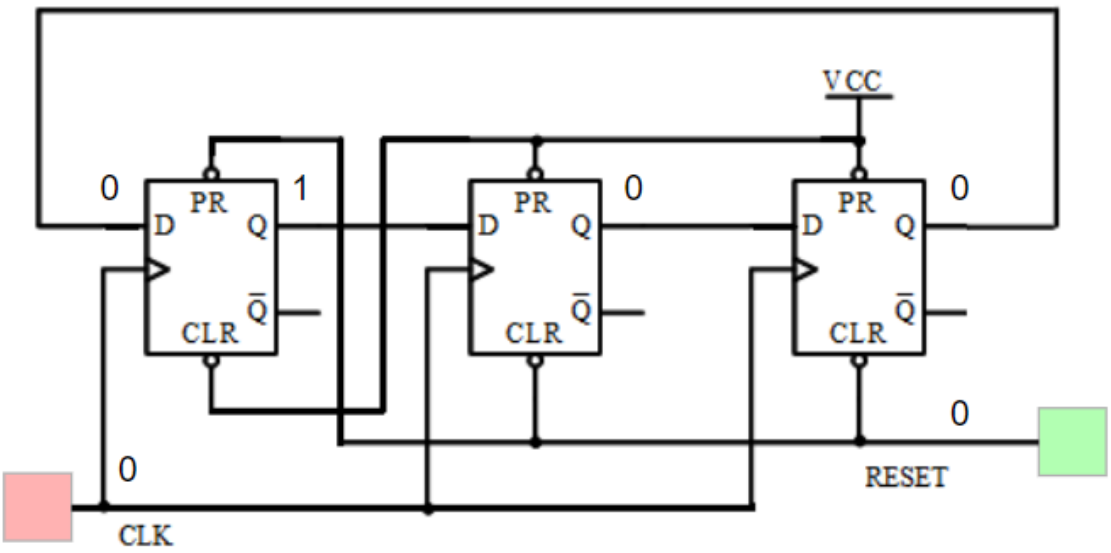
No. of states in Ring counter = No. of flip-flop used

Below is the block diagram of the 4-bit ring counter. Here, we use 4 D flip flops. The same clock pulse is passed to the clock input of all the flip flops as a synchronous counter. The **Overriding input (ORI)** is used to design this circuit.

The Overriding input is used as **clear** and **pre-set**.



OR



The output is 1 when the pre-set set to 0.

The output is 0 when the clear set to 0.

Both PR and CLR always work in value 0 because they are active low signals.

1. PR = 0, Q = 1
2. CLR = 0, Q = 0

These two values (always fixed) are independent with the input D and the Clock pulse (CLK).

Working:

The ORI input is passed to the PR input of the first flip flop, i.e., FF-0, and it is also passed to the clear input of the remaining three flip flops, i.e., FF-1, FF-2, and FF-3. The pre-set input set to 0 for the first flip flop. So, the output of the first flip flop is one, and the outputs of the remaining flip flops are 0. The output of the first flip flop is used to form the ring in the ring counter.

ORI	Clk	Q_0	Q_1	Q_2	Q_3
low	X	1	0	0	0
high	low	0	1	0	0
high	low	0	0	1	0
high	low	0	0	0	1
high	low	1	0	0	0

- ORI input set to low, and that time the Clk don't care.
- When the ORI input set to high, and the low clock pulse signal is passed as the negative clock edge triggered.

- A ring forms when the **pre-set 1** is shifted to the next flip-flop at each clock pulse.

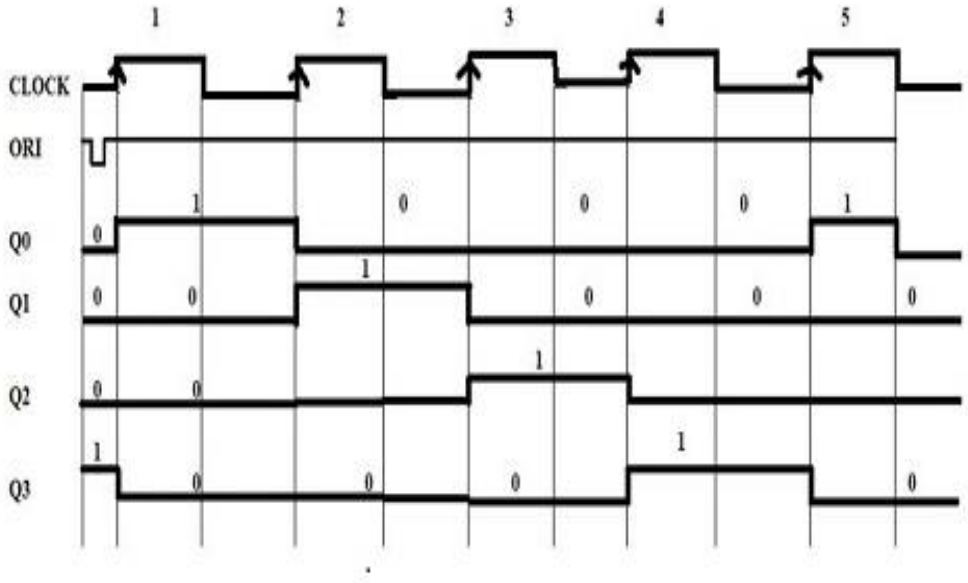
Procedure:

1.Set up the ring counter as per the following instructions.

Name of the Flip-Flop	Preset	Clear
FF-0	0	1
FF-1	1	0
FF-2	1	0
FF-3	1	0

2.Note down the state of the ring counter on the truth table for each clock pulse.

Output Waveforms:



Precautions:

1.Do not touch the pin of an IC and carefully insert the IC into the Bread board.

2.When inserting an IC into a bread board, be careful with the direction of the IC.

3.When installing an IC in the wrong direction, it might become damaged.

4.Since the storage temperature of an IC is between -20 ~ +70 degrees, keep it at room temperature, if possible.

5.When soldering an IC, solder it in as short a time as possible so that unnecessary heat is not applied to the device.

Result:

Conclusion:

Viva Questions:

1.What do you mean by Counter?

2.What are the types of Counters? Explain each.

3.What is the ring counter?

4.Why asynchronous counters are called as ripple counters?

5.What are the applications of synchronous counters?

Exp No: 08 **Date:**

Johnson Counter

AIM: Design a four-bit Johnson's counter using D Flip-Flops/JK Flip Flops and verify output.

Apparatus Required:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 7476/IC 7474	4/4
2	Bread board		1
2	Digital IC Trainer Kit	If required	1
3	Patch cards		REQUIRED
4	Power Supply	(0-5v)	1

Theory:

The Johnson counter is also known as twisted tail ring counter. In the ring counter we given the output of the last flip flop into the input of the first flip but in the Johnson counter the last flip flop complemented output is given to the input of the first flip flop. In this counter negative edge flip flop are used.

In Johnson counter the number of states is equal to twice the number of flip flops. If we use 4 flip flops, we will have 8 states so the number of the states are double. Another name of Johnson counter is creeping counter, twisted ring counter, walking counter, mobile counter and switch tail counter.

Note: The difference between the ring counter and Johnson counter is that it does not require pre-set.

Procedure:

1.Apply clock simultaneously to all flip flops.

2.Apply active low input to the clear pin of all flip-flops.

3. The output of the first flip flop which is Q0, is connected to the input of the second flip flop D1.

4. Output of the second flip flop which is Q1 is given to input of the third flip flop which is D2.

5. Output of the Third flip flop which is Q2 is given to input of the fourth flip flop which is D3.

6. The complemented output of the fourth flip flop which is $\bar{Q}_3$ is given to input of the first flip flop which is Do.

Circuit Diagram:

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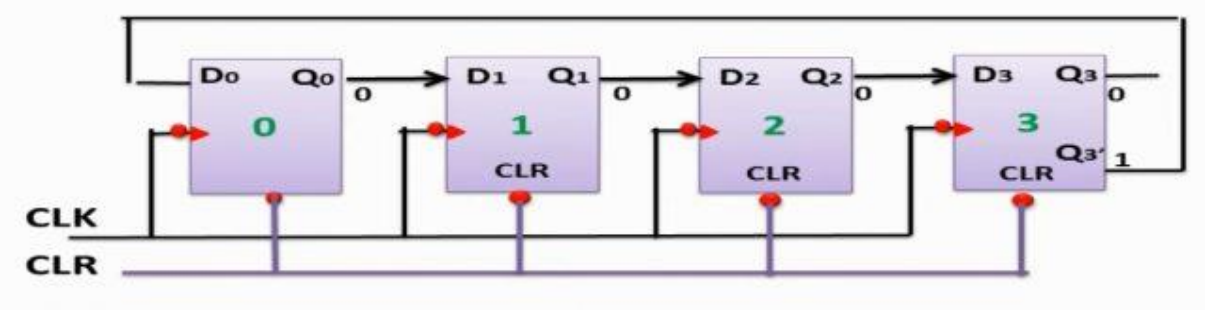
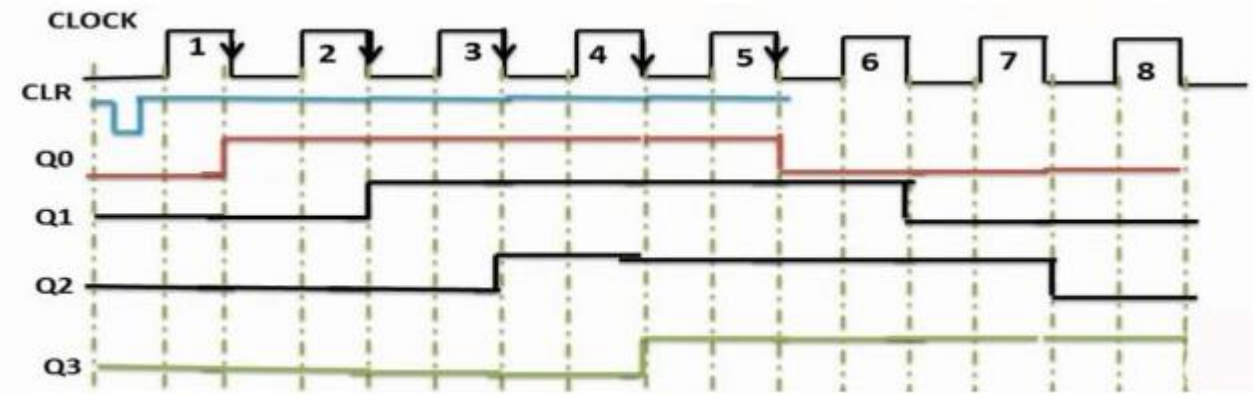


Truth Table:

Clear/ Pre-set	Clock	Qo	Q1	Q2	Q3
0	No clock	0	0	0	0
1	↓	1	0	0	0
1	↓	1	1	0	0
1	↓	1	1	1	0
1	↓	1	1	1	1
1	↓	0	1	1	1
1	↓	0	0	1	1
1	↓	0	0	0	1
1	↓	0	0	0	0

Timing Diagram or Output waveforms:



Precautions:

1.Do not touch the pin of an IC and carefully insert the IC into the Bread board.

2.When inserting an IC into a bread board, be careful with the direction of the IC.

3.When installing an IC in the wrong direction, it might become damaged.

4.Since the storage temperature of an IC is between -20 ~ +70 degrees, keep it at room temperature, if possible.

5.When soldering an IC, solder it in as short a time as possible so that unnecessary heat is not applied to the device.

Result:

Viva Questions:

1.Why Johnson counter is better than ring counter?
2. What is the difference between binary counter and Johnson counter?
3. What is the number of unused states in the Johnson counter?
4. What is the difference between ring and Johnson counter?
5. Consider a four-bit Johnson counter with an initial value of 0000.The counting sequence of this counter is **Ans: 0,8,12,14,15,7,3,1,0**

Exp No: 09 **Date:**

Universal shift register

AIM: Verify the operation of 4-bit Universal Shift Register for different Modes of operation.

Apparatus Required:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC 74291, IC 74395	4 4
2	Bread board		1
2	Digital IC Trainer Kit	If required	1
3	Patch cards		REQUIRED
4	Power Supply	(0-5v)	1

Theory: Shift registers are the sequential logic circuits that can store the data temporarily and provides the data transfer towards its output device for every clock pulse. These are capable of transferring/shifting the data either towards the right or left in serial and parallel modes. Based on the mode of input/output operations, shift registers can be used as a serial-in-parallel-out shift register, serial-in-serial-out shift register, parallel-in-parallel-out shift register, parallel-in parallel-out shift register. Based on shifting the data, there are universal shift registers and bidirectional shift registers. Here is a complete description of the universal shift register.

Universal Shift Register:

A register that can store the data and /shifts the data towards the right and left along with the parallel load capability is known as a universal shift register. It can be used to perform input/output operations in both serial and parallel modes. Unidirectional shift registers and bidirectional shift registers are combined together to get the design of the universal shift register. It is also known as a parallel-in-parallel-out shift register or shift register with the parallel load. Universal shift registers are capable of performing 3 operations as listed below.

- Parallel load operation – stores the data in parallel as well as the data in parallel
- Shift left operation – stores the data and transfers the data shifting towards left in the serial path
- Shift right operation – stores the data and transfers the data by shifting towards right in the serial path.

- Hence, Universal shift registers can perform input/output operations with both serial and parallel loads.

The design of a 4-bit universal shift register:

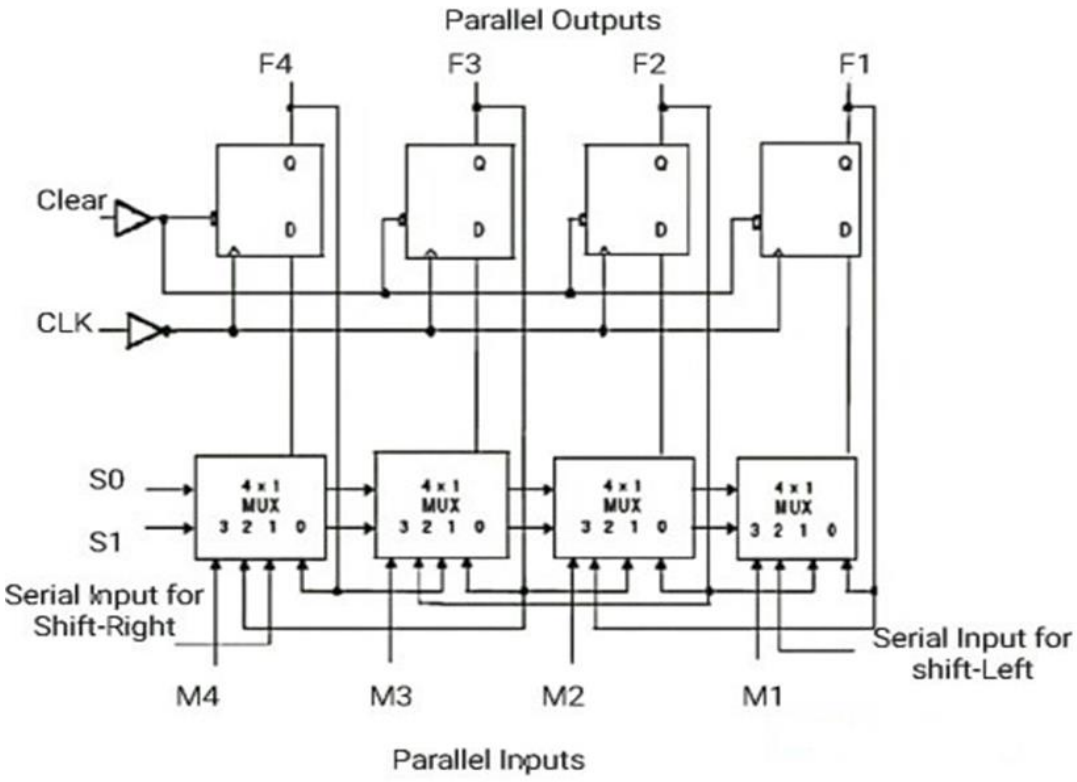


Figure:1 Universal shift register

Procedure:

- S0 and S1 are the selected pins that are used to select the mode of operation of this register. It may be shift left operation or shift right operation or parallel mode.
- Pin-0 of first 4×1 Mux is fed to the output pin of the first flip-flop. Observe the connections as shown in the figure.
- Pin-1 of the first 4X1 MUX is connected to serial input for shift right. In this mode, the register shifts the data towards the right.
- Similarly, pin-2 of 4X1 MUX is connected to the serial input for shift-left. In this mode, the universal shift register shifts the data towards the left.
- M1 is the parallel input data given to the pin-3 of the first 4×1 MUX to provide parallel mode operation and stores the data into the register.
- Similarly, remaining individual parallel input data bits are given to the pin-3 of related 4X1MUX to provide parallel loading.
- F1, F2, F3, and F4 are the parallel outputs of Flip-flops, which are associated with the 4×1 MUX.

Working of universal Shift Register:

- From the figure 1, selected pins decides the mode of operation of the universal shift register. Serial input shifts the data towards the right and left and stores the data within the register.
- Clear pin and CLK pin are connected to the flip-flop.
- M0, M1, M2, M3 are the parallel inputs while F0, F1, F2, F3 are the parallel outputs of flip-flops
- When the input pin is active HIGH, then the universal shift register loads / retrieve the data in parallel. In this case, the input pin is directly connected to 4×1 MUX
- When the input pin (mode) is active LOW, then the universal shift register shifts the data. In this case, the input pin is connected to 4×1 MUX via NOT gate.
- When the input pin (mode) is connected to GND (Ground), then the universal shift register acts as a Bi-directional shift register.
- To perform the shift-right operation, the input pin is fed to the 1st AND gate of the 1st flip-flop via serial input for shit-right.
- To perform the shift-left operation, the input pin is fed to the 8th AND gate of the last flip-flop via input M.
- If the selected pins S0= 0 and S1 = 0, then this register doesn't operate in any mode. That means it will be in a Locked state or no change state even though the clock pulses are applied.
- If the selected pins S0 = 0 and S1 = 1, then this register transfers or shifts the data to left and stores the data.
- If the selected pins S0 = 1 and S1 = 0, then this register shifts the data to right and hence performs the shift-right operation.
- If the selected pins S0 = 1 and S1 = 1, then this register loads the data in parallel. Hence it performs the parallel loading operation and stores the data.

S0	S1	Mode of Operation
0	0	Locked state (No change)
0	1	Shift-Left
1	0	Shift-Right
1	1	Parallel Loading

Precautions:

1.Do not touch the pin of an IC and carefully insert the IC into the Bread board.

2.When inserting an IC into a bread board, be careful with the direction of the IC.

3.When installing an IC in the wrong direction, it might become damaged.

4.Since the storage temperature of an IC is between -20 ~ +70 degrees, keep it at room temperature, if possible.

5.When soldering an IC, solder it in as short a time as possible so that unnecessary heat is not applied to the device.

Result:

Viva questions:

1. What are the types of loading the registers?
2. What do you mean by loading a register?
3. What are the basic types of shift registers?
4. What is a bidirectional shift register?
5. What do you mean by the storage capacity of a register?
6. What is a parallel-in, serial-out shift register?

Exp No: 10 **Date :**

MOD-8 RIPPLE COUNTER

AIM: Draw the circuit diagram of MOD – 8 ripple counter and construct a circuit using T-Flip-Flops and Test It with a low frequency clock and sketch the output waveforms.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC7474	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Asynchronous Counter:

A digital counter is a set of flip flop. An Asynchronous counter uses T flip flop to perform a counting function. The actual hardware used is usually J-K flip-flop connected to logic 1.

In ripple counter, the first flip-flop is clocked by the external clock pulse &then each successive flip-flop is clocked by the Q or /Q' output the previous flip-flop. Therefore in an asynchronous counter the flip-flop are not clocked simultaneously.

Up Counter:

Fig shows 3bit Asynchronous Up Counter. Here Flip-flop A act as a MSB Flip-flop and Flip-flop C can act as a LSB Flip-flop. Clock pulse is connected to the Clock of flip-flop C. Output of Flip-flop C (Qc) is connected to clock of next flip-flop (i.e. Flip-flop B) and so on. As soon as clock pulse changes output is going to –change (at the negative edge of clock pulse) as a Up count sequence. For 3 bit Up counter Truth table is as shown below.

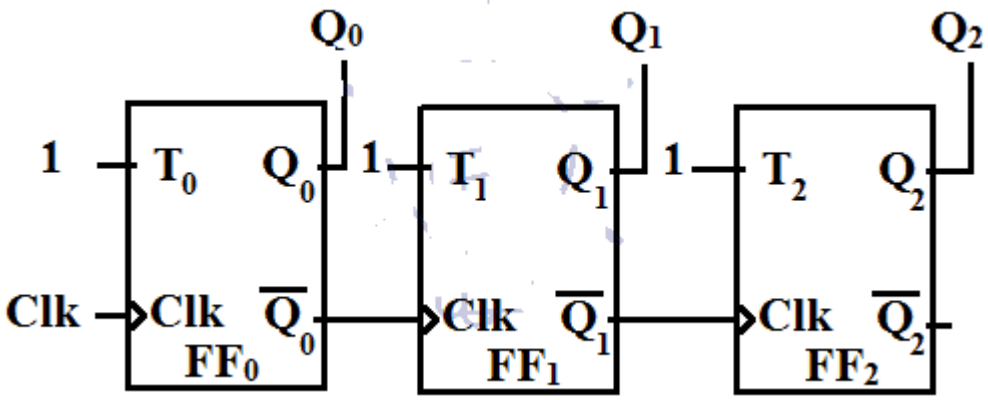
Down Counter:

Fig shows 3bit Asynchronous Down Counter. Here Flip-flop A act as a MSB Flip-flop and Flip-flop C can act as a LSB Flip-flop. Clock pulse is connected to the Clock of flip-flop C. Output of Flip-flop C (Qc') is connected to clock of next flip- flop (i.e. Flip-flop B) and so on. As soon as clock pulse changes output is going to change (at the negative edge of clock pulse) as a down count sequence. For 3 bit down counter Truth table is as shown below.

PROCEDURE:

Assemble the different counters as shown in above diagrams using JK flip-flop and verify its functionality by referring its function table.

Circuit Diagram of 3-Bit Ripple Up Counter:



Truth Table:

PRECAUTIONS:

1. Make the connections according to the IC pin diagram.
2. The connections should be tight.
3. The Vcc and ground should be applied carefully at the specified pin only.

RESULT:

VIVA QUESTIONS:

1. What do you understand by counter?
2. What is asynchronous counter?
3. What is synchronous counter?
4. Which flip flop is used in asynchronous counter?
5. Which flip flop is used in synchronous counter?

Exp No: 11 **Date:**

MOD–8 SYNCHRONOUS COUNTER

AIM: To Design MOD – 8 synchronous counter using T – Flip - Flop.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	IC7476	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

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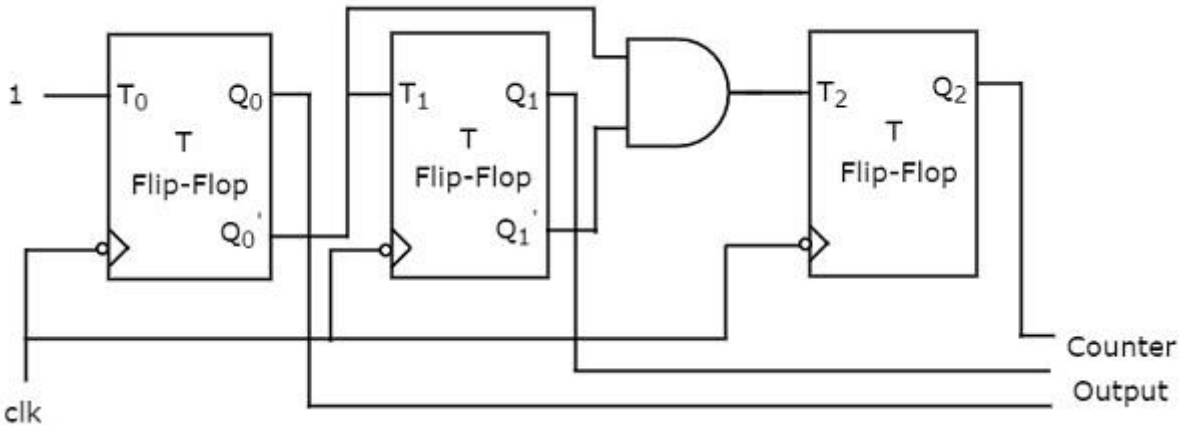
THEORY:

A counter in which each flip – flop is triggered by the output goes to previous flip - flop. As all the flip-flops do not change states simultaneously in asynchronous counter, spike occur at the output. To avoid this, strobe pulse is required. Because of the propagation delay the operating speed of asynchronous counter is low. This problem can be solved by triggering all the flip-flops in synchronous with the clock signal and such counters are called synchronous counters.

PROCEDURE:

- Check all the components for their working.
- Insert the appropriate IC into the IC base.
- Make connections as shown in the circuit diagram.
- Verify the Truth Table and observe the outputs.

BLOCK DIAGRAM OF MOD-8 COUNTER:



TRUTH TABLE:

RESULT:

VIVA QUESTIONS:

1. What are synchronous counters?
2. What are the advantages of synchronous counters?
3. What is an excitation table?
4. Write the excitation table for D, T - FF?
5. Design mod-5 synchronous counter using T-FF?

Exp No: 12(a) **Date:**

COMPARATOR

AIM: Draw the circuit diagram of a single bit comparator and test the output.

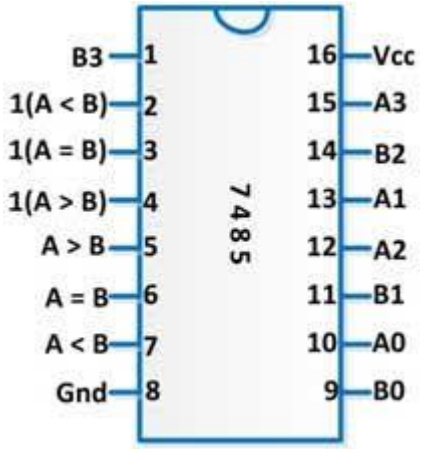
APPARATUSREQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	7485	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

THEORY:

Magnitude Comparator is a logical circuit, which compares two signals A and B and generates three logical outputs, whether A > B, A = B, or A < B. IC 7485 is a high speed 4-bit Magnitude comparator , which compares two 4-bit words . The A = B Input must be held high for proper compare operation.

PIN DIAGRAM:



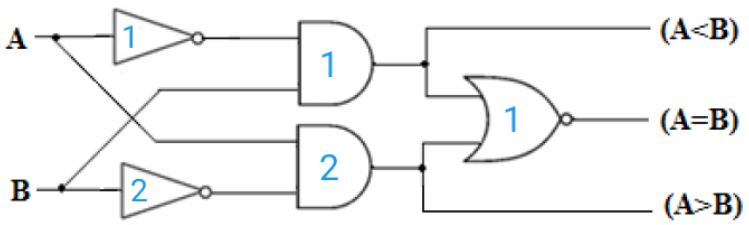


Fig. 1: One-bit Comparator

PROCEDURE:

1. Do the connection as per block diagram shown below and switch ON the power supply.
2. Give step by step inputs to A & B of comparator starting from MSB (A3and B3).
3. InitiallyjustobservethecomparisonbetweeninputsA&Binputsandignorethecascading inputs.
4. Once all possible combinations for A &B inputs are over then apply cascading inputs as per function table. Observe the outputs of comparator and verify it with function table.
5. Cascading inputs are used to increase the input line capacity of comparator.

TRUTH TABLE:

INPUTS		OUTPUTS		
A	**B**	**A<B**	**A=B**	**A>B**

RESULT:

VIVA QUESTIONS:

1. What are the applications of seven segment display?
2. Can you use the segments outputs of 7448 decoder directly to drive a 7-Segment LED? If not suggest a suitable interface?
3. Describe the operation performed by the decoder?
4. What is the function of RBI input?
5. What is the difference between common anode & common cathode display?

Exp No : 12(b) **Date:**

SEVEN SEGMENT DISPLAY

AIM: Construct 7-Segment Display Circuit Using Decoder and 7-Segment LED and test it.

APPARATUS REQUIRED:

S.NO	APPARATUS	RANGE	QUANTITY
1	IC	7447	1
2	Digital IC Trainer Kit		1
3	Patch cards		REQUIRED
4	Fixed Power Supply	(0-5v)	1

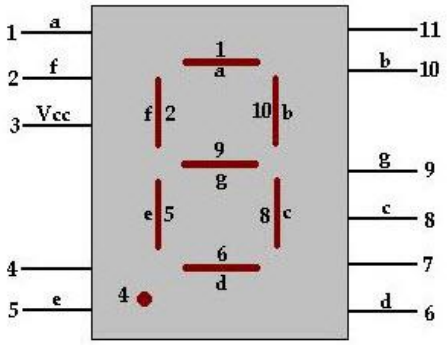
THEORY:

The functions of LT, RBI, RBO and BI are given below. LT this is called the LAMP TEST term in a land is used for segment testing. If it is connected to logic '0' level, all the segments of the display connected to the decoder will be ON. For normal decoding operation, this terminal is to be connected to logic '1' level. RBI For normal decoding operation, this is connected to logic '1' level. If it is connected to logic '0', the segment outputs will generate the data for normal 7- segment decoding, for all BCD inputs except Zero. Whenever the BCD inputs correspond to Zero, the 7-segment display switches off. This is used for zero blanking in multi-digit displays. BI Ifit is connected to logic '0' level, the display is switched-off irrespective of the BCD inputs. This is used for conserving the power in multiplexed displays. RBO This output is used for cascading purposes and is connected to the RBI terminal of the succeeding stage.

PROCEDURE:

1. Do the connection as per block diagram shown below and switch on the power supply.
2. For normal operation set LT = '1' RBI = '1' and BI/RBO = '1'. Apply input to the IC from I/P switches as per the function table and observe the output on seven segment display
3. You can give output of on board Decade counter (7490) as input to seven segment decoder. Observe the output on Display. It displays from 0 to 9 digits.
4. You can also give output of on board Binary counter (74191) as input to seven segment decoder. Observe the output on Display. It displays digits as shown in the function table for 0 to 15.

PIN DIAGRAM OF SEVEN SEGMENT DISPLAY:



TRUTH TABLE:

DECIMAL DIGIT	INPUT LINES				OUTPUT LINES						DISPLAY
0											
1											
2											
3											
4											
5											
6											
7											
8											
9											

RESULT:

VIVA QUESTIONS:

1. What is a comparator?
2. What are the applications of comparator?
3. Derive the Boolean expressions of one bit comparator and two bit comparators.
4. How do you realize a higher magnitude comparator using lower bit comparator ?
5. Design a 2-bit comparator using a single Logic gates?